MODEL QUESTION PAPER

MFCO2

I Semester M.TECH Examination, August 2011
ADVANCED COMPUTER SYSTEM ARCHITECTURE

Time: 3 Hours   Max. Marks: 75

GROUP A : Answer any three questions.

Q.1   Explain various modes of data transfer.
Q.2   Explain in detail locality of references.
Q.3   Explain the evaluation of Computers.
Q.4   Explain in detail about Tuning machine.
Q.5   Differentiate synchronous and Asynchronous data transfer.

GROUP B : Answer any three questions.

Q.6   Differentiate RISC and CISC.
Q.7   Explain Asynchronous Serial Transfer?
Q.8   List out various page replacement algorithms and define them.
Q.9   Explain advantages of synchronous communication, Discuss handshaking.
Q.10   Discuss the difference between tightly coupled and loosely coupled multiprocessors from the viewpoints of hardware organization and programming techniques.

GROUP C : All Questions are Compulsory.

Q.11   Fiil in the blanks

(i)   A typical cache block has _____bytes corresponding to eight 32-bit words.
(ii)   Program Counter (PC) is used for _____.
         _____ is a processor that performs computations on large arrays of data.
(iii)   RAID 0 is _____ storage.
(iv)   The main memory is sometimes called the _____.
(v)   A _____ is table, which is a pictorial representation of assigned address space for each chip in the system.

Q.12 Multiple choice question.

(i)   Limitations of Computers _____.
      (a) Unsolvable problems   (b) Intractable problems
      (c) Bath a & bl   (d) None.

(ii)   _____is simple computer technique for converting a long page number into a short one with fewer bits.
      (a) Hashing   (b) Paging
      (c) Segmentation   (d) None

(iii)   Register is _____ circuit.
      (a) Combinational   (b) Sequential
      (c) Both   (d) None of these

(iv)   In RISC processors, the branch instruction delays the pipeline operation until the instruction at the branch address is fetched.
      (a) Delayed operation   (b) delayed processing
      (c) Delayed branch   (d) delayed fetched

(v)   Mirroring is done in _____.
      (a) RAID 0   (b) RAID 5
      (c) Both   (d) None of these

Q.13 True or false

(i)   Cache is used as a high speed memory.
(ii)   An address of 24 lines can be access upto 2^{24} words of memory.
(iii)   Process is a single independent unit of program
(iv)   Jump is zero address instruction.
(v)   A multipart memory system employs separate buses between each memory module and each CPU.

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