MODEL QUESTION PAPER

MFET2

I Semester M.TECH Examination, August 2011
VLSI TECHNOLOGY AND PROCESS MODELING

Time: 3 Hours   Max. Marks: 75

GROUP A : Answer any three questions.

Q.1   Design a Bi-CMOS circuit for Z=A+BC.
Q.2   What are the limits on logic levels and supply voltage due tonoise?
Q.3   Explain Latch up effect in CMOS circuit in n-well structure.
Q.4   Construct a color-coded stick diagram to represent the design of the following integrated nMOS and CMOS structures and indicate pull up/ pull down ratios in a selectively lodable dynamic register to hold one four-bit word parallel

Q.5   List and explain scaling factors for device parameters (any five).

GROUP B : Answer any three questions.

Q.6   Explain write and read operation for dynamic and static memory cells with diagrams.
Q.7   Prove that Pg, Pa And Pt are scaled by $1/\beta^2$, α^2/β^2 and $1/\alpha^2\beta$, respectively.
Q.8   Explain the general arrangement of a 4-bit arithmetic processor.
Q.9   Explain the terms threshold voltage and threshold variation

Q.10   Draw and explain switch logic implementation of JK flip-flop.

GROUP C : All Questions are Compulsory.

Q.11 Fill in the blanks

(i)   Total Capacitance Ct = _____.
(ii)   Rise-time estimation for CMOS inverter is T_r=_____.

(iii)   A logical expansion of the p-well and n-well approaches is the _____ fabrication process.
(iv)   KCL determines _____ current.
(v)   Metal-Metal spacing is _____ than poly-poly spacing.

Q.12 Multiple choice question.

(i) What happens if DVDs is increased over saturation?
(a) Pinch-off   (b) Cut-off
(c) No change   (d) None of these

(ii) The colour code for n-diffusion is _____.
(a) Red   (b) Blue
(c) Green   (d) Yellow

(iii) Following scanning technique is used to reduce the test pattern geeration costs and also to reduce the test data and test time.
(a) Level sensitive scan design   (b) Built in self test.
(c) Boundary scan test   (d) Compact test.

(iv) Transconductance is measured in _____.
(a) Ohms   (b) Volts
(c) Amperes   (d) Mho or siemens

(v) $1/\beta$ is the scaling factor for supply voltage DVD and _____.
(a) Voss   (b) Parasitic capacitance
(c) Gate oxide thickness   (d) Channel length.

Q.13 True or false

(i) Gm for a bipolar transistor is Ic/kT/q.
(ii) CMOS technology has high input impedance.
(iii) Interlayer capacitance and Peripheral capacitance are the types of Area capacitance.
(iv) Bipolar devices are low voltage swing devices.
(v) The p-channel MOS consists of lightly doped substrate of n - type silicon material.

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